Docket No.: RSW920030255US1 (7161-141U) **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 46320
Martin PRESLER-MARSHALL	:	Confirmation Number: 7476
Application No.: 10/759,410	:	Group Art Unit: 2186
Filed: January 16, 2004	:	Examiner: R. Dare
For: SELF TUNING CACHE	:	

REQUEST FOR PRE-APPEAL BRIEF REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request that a Panel Review of the rejected claims in the final Office Action dated September 6, 2006, be performed in the above identified application.

CLAIMS 1-6, 8-9, 11, 13-16, 18-19, 21, AND 23-25 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY LAHIRI ET AL., U.S. PATENT NO. 6,952,664 (HEREINAFTER LAHIRI)

On pages 2 and 3 of the Response filed June 1, 2006, Applicant argued that the Examiner failed to establish that Lahiri identically discloses that "a second one of said test caches having a cache size which is greater than said size of said primary cache." The operational buffer of Lahiri has a 2 gigabyte size, whereas the cache simulator, which contains each of the segments, only has a size of 40 megabytes. Since the caches are "simulated" using the segments, certain of the segments (although possibly having a simulated size twice that of the operational cache) do not have, in actuality, a size greater than the size of operational cache.

The Examiner's response to this argument is found on page 11 of the Office Action, in which the Examiner asserted:

> The term cache size, as used by Applicant and Lahiri refers to the number of entries/buffers in a cache. The cache size is not the size of the database environment in which the cache simulation system exists as Applicant suggests, quoting col. 5 line 64 through col. 6, line 3 of Lahiri. Col. 3, lines 49-55, among other places in Lahiri reference, equates cache size with the number of entries. Since one of the simulated caches has more entries/buffers that the primary cache, Lahiri does teach a test cache with a cache size greater than the primary cache.

Although the Examiner cited column 3, lines 49-55 for support of the Examiner's assertion that cache size is "the number of entries/buffers in a cache," this cited passage neither mentions entries nor buffers. Applicant also notes that the Examiner did not cite any passage within Applicant's disclosure to support the Examiner's assertion.

On the contrary, column 5, lines 64-65 of Lahiri teaches "the operational buffer cache may be two gigabytes in size" (emphasis added). Thus, Lahiri specifically teaches that size of a cache is measured in terms of bytes, not buffers. Thus, the Examiner's assertion with regard to how one having ordinary skill in the art would interpret the phrase "cache size" is directly contradicted by Lahiri.

Moreover, as noted above, Lahiri doesn't teach claimed "second one of the test caches" because the these asserted caches are "simulated." A simulated cache is not a subset of caches just as a simulated tree is not a subset of trees. As another example, a drawing of a computer is a "simulated computer;" however one having ordinary skill in the art would not recognize that drawing as a computer.

Therefore, for the reasons stated above, Applicants submit that the Examiner has failed to establish that Kheirolomoom identically discloses the claimed invention, as recited in claims 1-4 and 6-11, within the meaning of 35 U.S.C. § 102.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 09-0461, and please credit any excess fees to such deposit account.

Date: December 5, 2006

Respectfully submitted,

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